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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,078	PECK, JOSEPH E.	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/06/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected t o by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed 8/6/2003.

Claims 1-39 have been submitted for examination.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 6 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 85 of U.S. Patent No. 7,024,660 (hereinafter '660). Although the conflicting claims are not identical, they are not patentably distinct from each other because the following observations.

As per instant claim 6, '660 claim 85 also recites computer medium with program comprising converting a first hardware configuration program (HCP) deployable onto the programmable hardware element (PHE) to perform first portion of the function (see claim 85:

the hardware configuration program ... deployable on a programmable hardware element ... implements the function); configuring the PHE with the first HCP (*wherein the hardware configuration program ... specifies usage of ... hardware resources by the programmable hardware element in performing the function*); the PHE executing the first portion of the function (*'...for the programmable hardware element that implements the function*' ; OR '*test configuration ... deploy test configuration onto the programmable hardware element ... after configuration ... provides for communication ... hardware resources and the program'*). Unlike claim 6, '660 claim 85 does not explicitly recite 'the computer system executing the remaining portion of the program, this remaining portion operable to be analyzed and debugged in response to said executing and receiving user input modifying said remaining portion to debug said portion' and 'invoking one or more hardware resources to perform the function' with the PHE being coupled to said one or more hardware resources (*). However, claim 85 recites *"... for debugging purposes ... by a processor ... to test performance of the function... hardware resources ... program communicates with ... resources ... through the programmable hardware element*' along with '*the programmable hardware element ... after configuration ... provides for communication ... hardware resources and the program*' (i.e. the very program of claim 6 as being the *user interface to receive user input specifying the function,* whose performance is analyzed and tested via the PHE communicating with the one or more hardware resources (of claim 85). This additional debugging by a computer processor to monitor the performance of the PHE (implementing a specified function) being configured with and coupled to additional *fixed* hardware resources and communicate with the main program **reads on** this *remaining portion* of the user debug program. Although the language of the limitations appear non identical, in light

of the above recital by '660 claim 85, the teachings of claim 85 amount to what is deemed, by one skill in the art, non-distinct or equivalent in terms of limitation or features to what is recited above as (*) in claim 6 in a anticipatory fashion.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Tseng et al., USPN: 6,009,256 (hereinafter Tseng).

As per claim 1, Tseng discloses a memory medium comprising program instructions for debugging a program, wherein the program is intended for deployment on a programmable hardware element (e.g. Fig. 7-8; col. 4, lines 42-50; Fig. 22-33) to perform a function, wherein the program instructions are executable to perform:

a) converting a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function (e.g. *hardware model 20* - Fig. 1; Fig. 6; Fig. 27-31; col. 11, lines 47 to col. 12, line 19; step 125- Fig. 2), wherein a remaining portion of the program is to be debugged by a user (step 140 – Fig. 2);

b) configuring the programmable hardware element with the first hardware configuration program (col. 11, lines 47 to col. 12, line 19);

c) executing the program, wherein said executing comprises: the programmable hardware element executing the first portion of the program (step 125- Fig. 2); and the computer system executing the remaining portion of the program; wherein the remaining portion of the program is operable to be analyzed and debugged in response (e.g. col. 35, line 65 to col. 36, line 50) to said executing; and

d) receiving user input modifying the remaining portion of the program to debug the remaining portion of the program (e.g. col. 12, line 20-42).

As per claim 2, Tseng discloses wherein the program instructions are further executable to implement: repeating a)-d) one or more times, wherein in each iteration of a)-d) the first portion of the program is a successively larger portion of the program (e.g. Fig. 5; col. 15, lines 34-57).

As per claim 3, Tseng discloses: repeating a)-d) a plurality of times; wherein, in a first subset of iterations of a)-d) the first portion of the program is a successively larger portion of the program; and wherein, in a second subset of iterations of a)-d) the first portion of the program is a successively smaller portion of the program (re claim 2 – Note: loop back into the simulation process using actual analysis results reads on successively creating larger portions of starting program; wherein each subset of actions taken per iteration reads on successively smaller portion that the whole SIM/Emualtion program – see Fig. 2, 5; col. 35, line 65 to col. 36, line 50).

As per claim 4, Tseng discloses implementing after the program has been debugged, converting the program into a second hardware configuration program which is deployable on the programmable hardware element to perform the function; and configuring the programmable

hardware element with the second hardware configuration program (step 115, step 150 – Fig. 2; *step 339/YES → step 332→334, Update Registers, modeled in hardware*, step 337 – Fig. 5).

As per claim 5, Tseng discloses wherein said converting the first portion of the program into a first hardware configuration program comprises receiving user input (step 304 – Fig. 3; col. 18, line 47 to col. 19, line 13) indicating the first portion of the program.

As per claims 6-7, Tseng discloses wherein the programmable hardware element is coupled to one or more hardware resources, and wherein said executing further comprises: invoking the one or more hardware resources to perform the function (e.g. *REG1, S2, Q1* - Fig. 22-24, 26-33); wherein the program is specified to access the one or more hardware resources, and wherein the program instructions are further executable to perform:

prior to said configuring the programmable hardware element with the first hardware configuration program, analyzing the remaining portion of the program and the one or more hardware resources (Fig. 5);

determining a test feed-through configuration based on said analyzing, wherein the test feed-through configuration is deployable on the programmable hardware element (PHE) to provide for communication between the remaining portion of the program and the one or more hardware resources (Post analysis step 140 – Fig. 2 – Note: post analysis leading to step 120 reads on deployable on the PHE to iterate on more loop); and

including the test feed-through configuration in the first hardware configuration program; wherein said configuring the programmable hardware element with the first hardware configuration program further comprises configuring the programmable hardware element with the test feed-through configuration (step 332-339 – Fig. 5); and

wherein said executing the remaining portion of the program further comprises the remaining portion of the program communicating with the one or more hardware resources through the programmable hardware element (Fig. 22-33).

As per claims 8-9, Tseng discloses wherein the program instructions are further executable to implement: repeating a)-d) one or more times, wherein in each iteration of a)-d) the first portion of the program is a successively larger portion of the program (refer to claim 3); wherein in each iteration of a)-d), said determining a test feed-through configuration and said including the test feed-through configuration in the first hardware configuration program are performed only if the remaining portion of the program is specified to access the one or more hardware resources (see Fig. 2, Fig. 5 as per rationale explained in claim 4).

As per claim 10, Tseng discloses wherein in each iteration of a)-d), said determining the test feed-through configuration comprises modifying (step 335 – Fig 5; col. 9, lines 61-67) the test feed-through configuration based on said analyzing the remaining portion of the program.

As per claim 11, refer to claim 3

As per claims 12-14, Tseng discloses determining the one or more hardware resources; receiving user input indicating the one or more hardware resources; querying the one or more hardware resources (e.g. Fig. 22-24, 26-33; col. 36, lines 13-40).

As per claim 15, Tseng discloses determining a plurality of pre-compiled hardware configuration program components; and assembling the plurality of pre-compiled hardware configuration program components, thereby generating the test feed-through configuration (e.g. *modeled in hardware (except memories)* -- step 332-337 – Fig. 5).

As per claim 16, Tseng discloses wherein said determining the test feed-through configuration comprises: generating a test feed-through software program based on said analyzing; and compiling the test feed-through software program, thereby generating the test feed-through configuration (e.g. col. 5, lines 45-51 – Note: providing input to a model and simulating based on the modified model reads on compile via feed-through for generating more simulation test results – see Fig. 5).

As per claim 17, Tseng discloses storing the test feed-through configuration on the computer system, wherein the stored test feed-through configuration is retrievable for use in other reconfigurable systems (e.g. *logging selective input ... output* – col. 5, lines 40-51; col. 36, lines 20-48 – Note: recording results in log to be able to use for further testing from a point onward reads on retrievable for use by other systems – as in *bench marks* – col. 60, lines 53-62) using the one or more hardware resources.

As per claim 18, Tseng discloses determining a plurality of pre-compiled hardware configuration program components; assembling the plurality of pre-compiled hardware configuration program components, thereby generating a first portion of the test feed-through configuration; generating a test feed-through software program based on said analyzing; compiling the test feed-through software program, thereby generating a second portion of the test feed-through configuration; and combining the first portion of the test feed-through configuration and the second portion of the test feed-through configuration, thereby generating the test feed-through configuration (refer to claim 16 because of analogous sequences of steps)

As per claims 19-20, Tseng discloses a subset of the one or more hardware resources comprises one or more hardware cartridges like an I/O cartridge (Fig. 22-29 – Note: I/O data

collecting entities being manipulated by user via the HDL design reads on a measurement entity -- like a gate or a register -- being not fixed and physically removed via disconnection by the modeling act of the user).

As per claims 21-22, Tseng discloses wherein the first portion of the program comprises a substantially debugged portion of the program; wherein the computer system executing the remaining portion of the program simulates execution of the remaining portion of the program on the programmable hardware element (see Fig. 2; col. 35, line 65 to col. 36, line 50 in light of corresponding mapping rationale in claim 1).

As per claim 23, Tseng discloses a memory medium comprising program instructions for debugging a program, wherein the program is usable to configure a reconfigurable system, wherein the program performs a function, wherein the reconfigurable system includes a programmable hardware element, wherein the program is intended for deployment on the programmable hardware element, wherein the program instructions are executable to perform:

a) receiving user input indicating a first portion of the program for deployment on the programmable hardware element (e.g. *hardware model 20* - Fig. 1; Fig. 6; Fig. 27-31; col. 11, lines 47 to col. 12, line 19; step 125- Fig. 2 – Note: modeling w/ HDL and RTL connectivity reads on user input), wherein a remaining portion of the program is to be debugged by a user;

b) converting the first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function;

c) configuring the programmable hardware element with the first hardware configuration program;

d) executing the program, wherein said executing comprises: the programmable hardware element executing the first portion of the program; and the computer system executing the remaining portion of the program; wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing; and

e) receiving user input modifying the remaining portion of the program to debug the remaining portion of the program;

wherein steps b) → e) have been addressed with the corresponding mapping as set forth in claim 1.

As per claims 24-26, refer to claims, 4, 2-3, respectively.

As per claim 27, Tseng discloses a memory medium comprising program instructions for debugging a program, wherein the program is usable to configure a reconfigurable system, wherein the program performs a function, wherein the reconfigurable system includes a programmable hardware element, wherein the program is intended for deployment on the programmable hardware element, wherein the program instructions are executable to perform:

receiving (user input indicating a first portion of the program for deployment … wherein a first remaining portion …);

converting (the first portion … a first hardware configuration program which is deployable … programmable hardware element …);

configuring (the programmable hardware element with the first …);

executing the program, (… the programmable hardware element executing the first portion of the program… computer system executing the first remaining portion of the program;

wherein the remaining portion ...receiving user input ...debug the remaining portion of the program); all of which limitations having been addressed in claim 23 above.

Tseng further discloses

receiving user input indicating a second portion of the program for deployment on the programmable hardware element, wherein the second portion of the program comprises the first portion of the program and a debugged portion of the first remaining portion of the program,

wherein a second remaining portion of the program is to be debugged by a user, wherein the second remaining portion comprises only a subset of the first remaining portion of the program;

converting the second portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function;

configuring the programmable hardware element with the first hardware configuration program; executing the program, wherein said executing comprises: the programmable hardware element executing the second portion of the program; and the computer system executing the second remaining portion of the program. (refer to claims 2-3 – Note: all of which fall under the steps repetition subject matter of claims 2-3; hence would have to be referred to claim 2 or 3).

As per claim 28, Tseng discloses a system for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, the system comprising: a reconfigurable device, comprising: a programmable hardware element; and a computer system comprising a processor and a memory; wherein the computer system is

coupled to the reconfigurable device (e.g. Fig. 1; Fig. 7-8; col. 4, lines 42-50; Fig. 22-33); wherein the memory stores program instructions which are executable by the processor to :

a) convert ...; b) configure ...;

c) execute ...; and d) receive user input ...;

wherein the steps are exactly as recited in claim 1.

The steps will be rejected as set forth in claim 1.

As per claims 29-31, refer to claims 2-4, respectively.

As per claim 32, this is the system for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, comprising means for performing the same steps as recited in claim 1; and these steps are rejected as set forth correspondingly in claim 1.

As per claims 33-35, these are system claims corresponding to claims 2-4, respectively; and their rejection are referred thereto, respectively.

As per claim 36, refer to the method for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, comprising:) convert ...; b) configure ...; c) execute ...; and d) receive user input ...; as recited in claim 1 for corresponding rejection.

As per claims 36-39, these are system claims corresponding to claims 2-4, respectively; and their rejection are referred thereto, respectively.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence – please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan A Vu
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October 15, 2006